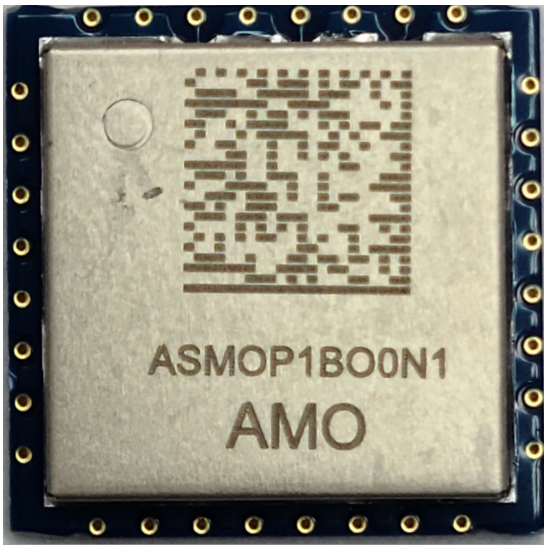
AMO UWB Module(SR150)

Rev 0.9

(ASMOP1BO0N1)



Revision	Contents	Date
0.1	New	26th, October, 2020.
0.9	Revision	23th, June, 2021

23th, June, 2021

AMOSENSE Co., LTD.

Notes

The contents of this data sheet are subject to change without notice. Please confirm the specifications and delivery conditions when placing your order.

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1. Introduction

The UWB module is based on NXP's SR150 Ultra Wideband (UWB) transceiver IC. It integrates all RF circuitry, power management and clock circuitry in one module compliant to IEEE 802.15.4 HRP UWB PHY.

It can be used for 2-way ranging measurement and TDoA based one way ranging.

Embedded PHY and MAC compatible with FiRa consortium specification

1.1 Key Features

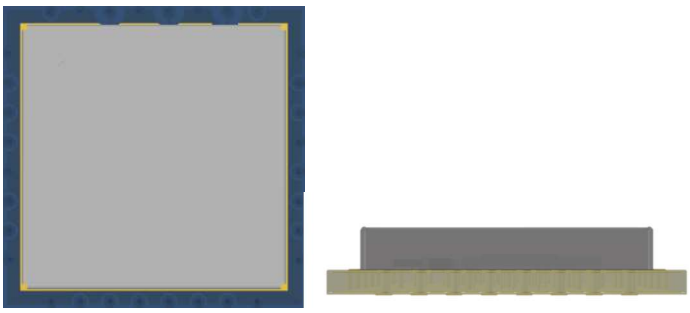
AMO UWB SR150 Module	
	
ANT Type	• External Antenna
Size	• 13mm x 13 mm x 2.7mm
Interface	• Host interface is SPI, Secure element interface is I2C
Main ICs	• SR150, ARM® Cortex-M33 32 Bit processor (SR150 is not customer programmable so these flash and RAM/ROM are not available to end customer.)
Reference Clocks	• 38.4MHz clock • 32.768KHz clock
Frequency Band	• 6.24 GHz ~ 8.24 GHz
Supply Voltage	• 3.0 to 3.6 (Typ. 3.3) V
Output Power	• MAX +12 dBm
Package	• Metal Shield CAN

Table 1. Key Features

* Shield CAN size : 11.5mm x 11.5mm x 1.65mm

1.2 Applications

① IOT applications
② Consumer devices
③ Smart home devices
④ RTLS anchor etc.

2. Part Numbering

[Example]

Device Family

AS MO P 1B O 0 N 1

Company name

AS = AMOSENSE

Device type

MO = Module, **DT** = Tag, **DA** = Anchor

Type

P = PCB, **F** = FPCB, **K** = Package

Chipset

1B = SR150, **1C** = SR040

Configuration

O = UWB Only, **B** = UWB + BLE(MCU), **M** = UWB + MCU

MCU Part number

0 = UWB Only, **1** = QN9090

Antenna

N = Non, **A** = Antenna, **R** = Receptacle, **S** = SMA

Version

1

Note : Provisional designation

3. Module Block Diagram

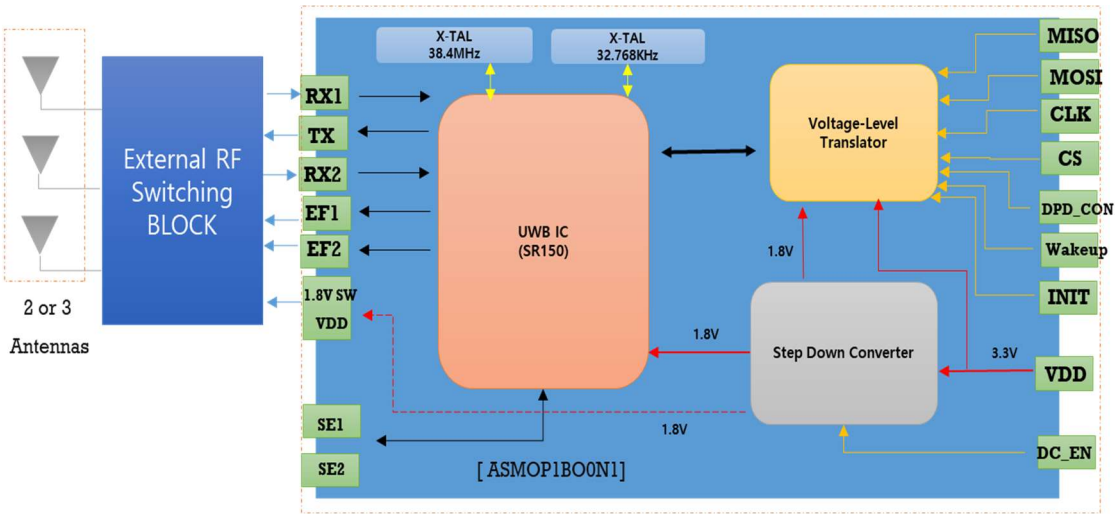


Figure 1. Block Diagram of AMO UWB Module

4. Module Characteristics

4.1 Electrical Characteristics

Parameter	Min	Typ.	Max	Unit
Supply Voltage(VDD)	3.0	3.3	3.6	V
Current Consumption			180	mA
Operating Temperature	-30	25	+85	˚c
RF Input Power	-	-	7	dBm
ESD (Human Body Model)			2000	V

Table 2. Electrical Characteristics

4.2 RF Characteristics

- T = 25°C, VDD = 3.3 V (typ.)

Parameter	Condition	Min	Typ.	Max	Unit
Frequency Range		6.24	-	8.24	GHz
TX Output Power	CW		12		dBm
	CH5 during preamble peak		10.5		
	CH9 during preamble peak		11.5		
Data Rate		0.85	6.8	31.2	Mbps
AOA accuracy	SNR ≥ 34dB at input	-3		+3	Deg
	26dB ≤ SNR < 36dB at input	-10		+10	
ToF accuracy	LOS when STS is used	-10		+10	Cm
	NLOS when STS is used	-20		+20	
RF Sensitivity	Single / 6.8 Mbps		-93		dBm
	Dual / 6.8 Mbps		-94		

Table 3. RF Characteristics

5. Power Up

SR150 Module has a main power up sequence that require VDD.
High level boot sequence is indicated below, when voltages are settled down CE can be asserted along with VDD within 50us, else design will transition to HPD state.

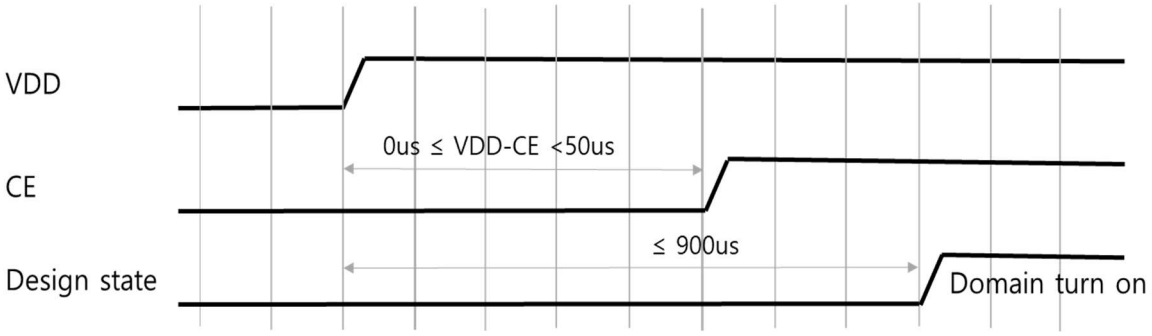


Figure 2. power up sequence

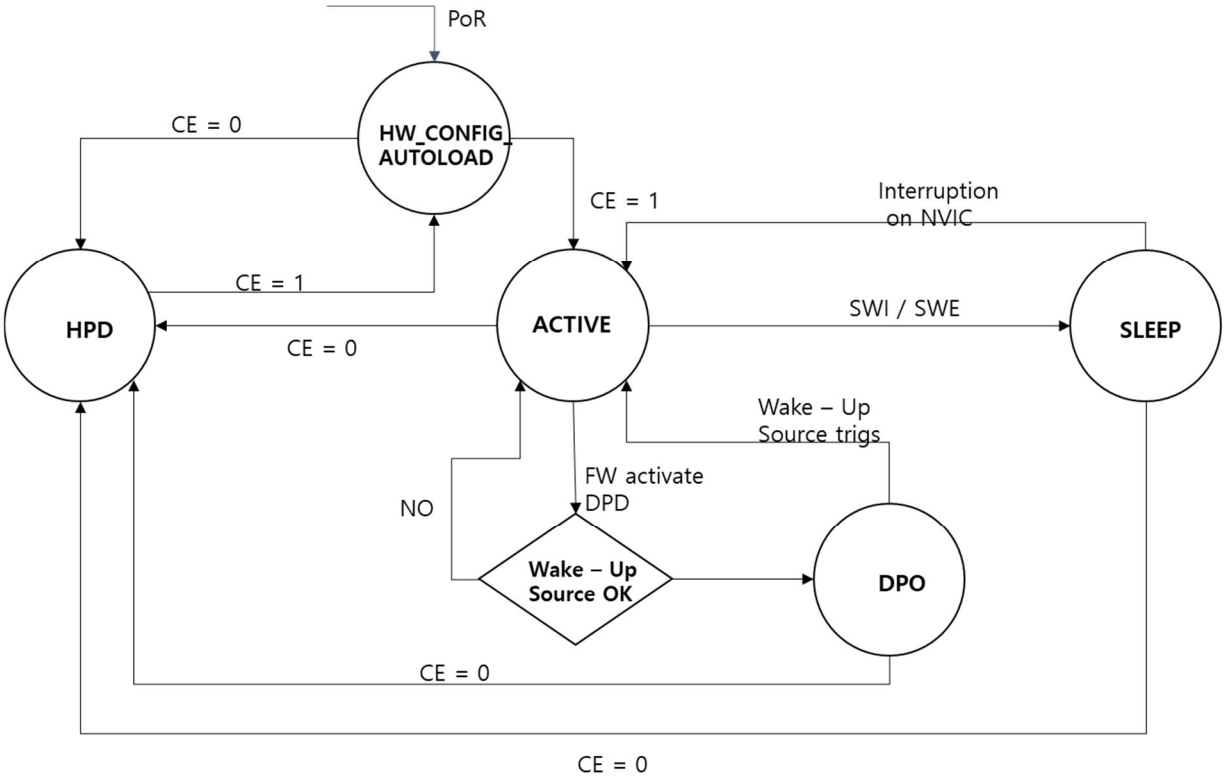


Figure 3. SR150 power modes state diagram

6. SYSTEM MODES

The SR150 Module has 6 power modes that are specified: Host power down mode, Deep power down mode, Deep power down retention mode, Sleep, Active mode and Hardware configuration Autoload. A description of the states can be found in Table 4

System power state	Description
Active mode	The device is running and supplied by the Platform PMU, in this mode several active states are available: Idle, TX, RX and Dual RX
Deep power down mode (DPD)	The device is in low power mode and supplied by the Platform PMU, the memory are not supplied, a configured wake up can bring the device back to the Active mode, for this a firmware reload is necessary, no RF communication is possible
DPD retention mode	The device is in deep power down mode but the memory is supplied
Sleep	Specific parts can be active or inactive, this sleep mode can be configured by firmware which enables several power states, no RF communication is possible
Hard power down mode	The device is powered down and supplied by the PMU, it can by activated by the chip enable signal
Hardware configuration Autoload	The devices is supplied by the platform PMU and is loading the Hardware configuration and firmware into the memory

Table 4. System Power states description

The time required for SR150 to go into DPD from is <100us controlled by the firmware.
Similarly, the required time for SR150 to enter HPD state is less than 100us starting for the instance that CE is de-asserted. The Wakeup timing from DPD state is around 370 us, the wakeup form HPD state is triggered once CE is asserted and takes around 380us.

7. SPI Host Interface

SPI-bus Master/Slave interface, up to 20 Mbits/s

Features
- Synchronous, Serial, Full-Duplex communication, up to 16.66 Mbits/s
- Data frames of 8-bits and 16bits supported
- Programmable clock polarity and phase
- LSB/MSB first order
- Programmable SSEL polarity

SPI-bus configuration options In order to select SPI-bus interface for host communication, the host interface choice and settings are programmed during production. The SPI-bus IP supports four operating modes selectable using SPInCfg register. The operation mode of the SPI-bus is shown in Table 5, CPHA refers to the Clock Phase option and CPOL refers to the Clock Polarity.

Connection
CPHA switch: Clock Phase: defines the sampling edge of MOSI data • CPHA = 1: data are sampled on MOSI on the even clock edges of SCK after NSS goes low • CPHA = 0: data are sampled on MOSI on the odd clock edges of SCK after NSS goes low
CPOL switch: Clock Polarity • CPOL = 0: the clock is idle low and the first valid edge of SCK will be a rising one • CPOL = 1: the clock is idle high and the first valid edge of SCK will be a falling one

Table 5. SPI-bus configuration

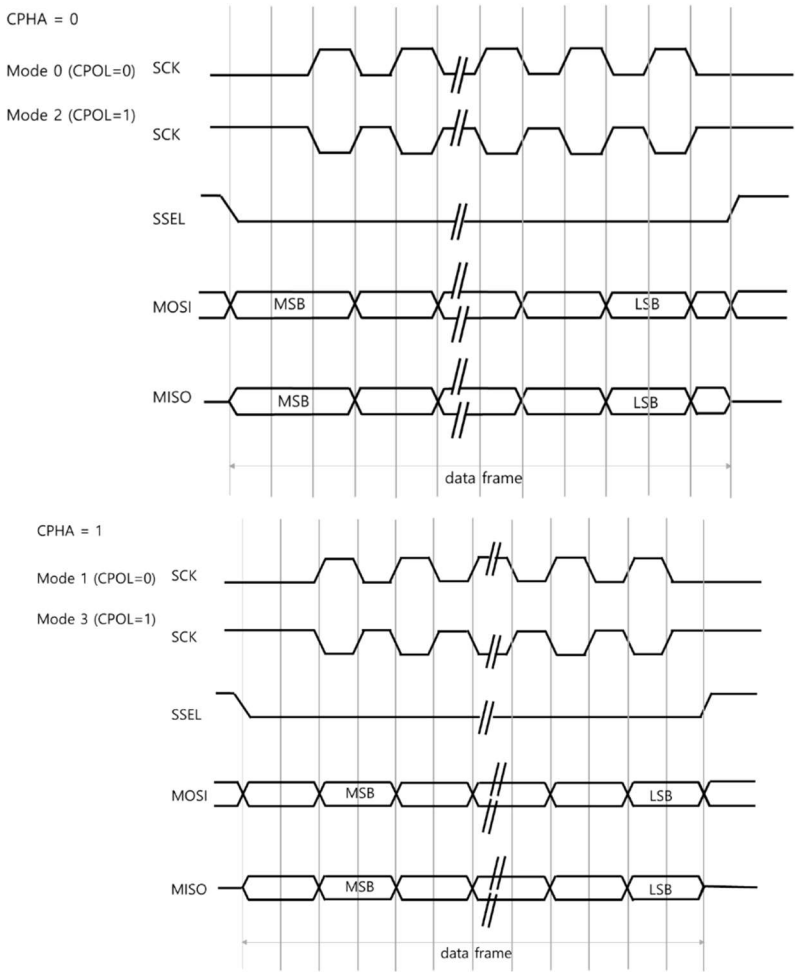


Figure 4. SPI date frame

The SPI-bus interface shares the pins with the other host interfaces that are supported by SR150. When SPI-bus is configured the functionality of the interface pins is as described in Table 6.

When a master device transmits data to the SR150 via the MOSI line, the SR150 responds by sending data to the master device via the MISO line. This implies full-duplex transmission with both, data out and data in synchronized with the same clock signal.

SR150 starts sampling when receiving a logic low at pins NSS Host_2 pin and the clock at input pin HOST_1. Thus, SR150 is synchronized with the master. Data from the master is received serially at the slave MOSI line and loaded in the 8-bit shift register.

After the 8bit shrift register is loaded, its data is transferred to the read buffer. During a write cycle, data is written into the shift register, then the SR150 waits for a clock train form the master to shift the data out on the MISO line.

Both master and slave devices must operate with the same timing. The master device always places data on the MOSI line a half cycle before the clock edge SCK, for the slave device to latch the data.

Pin	functionality	HW connection when used	HW connection when NOT used
Host conntection			
Host_1	SCK (Serial input Clock)	host	Must be connected
Host_2	NSS (Not Slave Select)	host	Must be connected
Host_3	MOSI (Master Out Slave In) Data input	host	Must be connected
Host_4	MISO (Master In Slave Out) Data output	host	Must be connected
GPIO05_SENSORINT	IRQ sent to the Host to let it know data are available for read	host	Must be connected
CHIP_EN	connection for the HOST to disable/enable the chip	host	Must be connected
RTC_SYNC	TBD	TBD	TBD
GPIO03_WAKEUP	SPI Rx Handshake from Host to SR150	host	Must be connected

Table 6. the functionality of the interface pins

8. Secure Element (SE) interface

I2C Connections with SE for secure ranging are described below.

Pin	functionality
SE_SCL	SCL 10k pull up to VDD 1V8 to be tune according to I2C line shape analysis
SE_SDA	SDA (secure keys generated by SE exchange) 10k pull up to VDD 1V8 to be tune according to I2C line shape analysis
GPIO/SE_INT	Host Secure Element interrupt (IRQ flag to indicate that data are ready to be shared via I2C)

Table 7. Secure Element (SE) interface

9. Antenna switch control GPIOs

Specific GPIOs are used for antenna switching. Fast switching antenna capability must be available offering the capability to switch the antenna between transmitted packets.

Pin	Supply reference	functionality
EF1 EF2	VDD_IO	High switching speed general purpose IO used for antenna external switches, switching time is dependent on the end control point, 125ns when controlled by ARM, 33ns when controlled by the DSP

Table 8. Antenna switch control GPIOs

10. RF connections

SR150 has 2 RF inputs (RX1, RX2) and one RF output (TX). These 3 RF ports can be connected to 2 or 3 antennas. As TX and RX2 share one antenna, an RF SPDT switch is needed. The same RF switch is therefore implemented on RX1 path to guarantee the same path characteristics (insertion loss, electrical delay).

Below schematic depicts the connection from SR150 to the antenna. In this configuration ranging and 2D AoA are fulfilled.

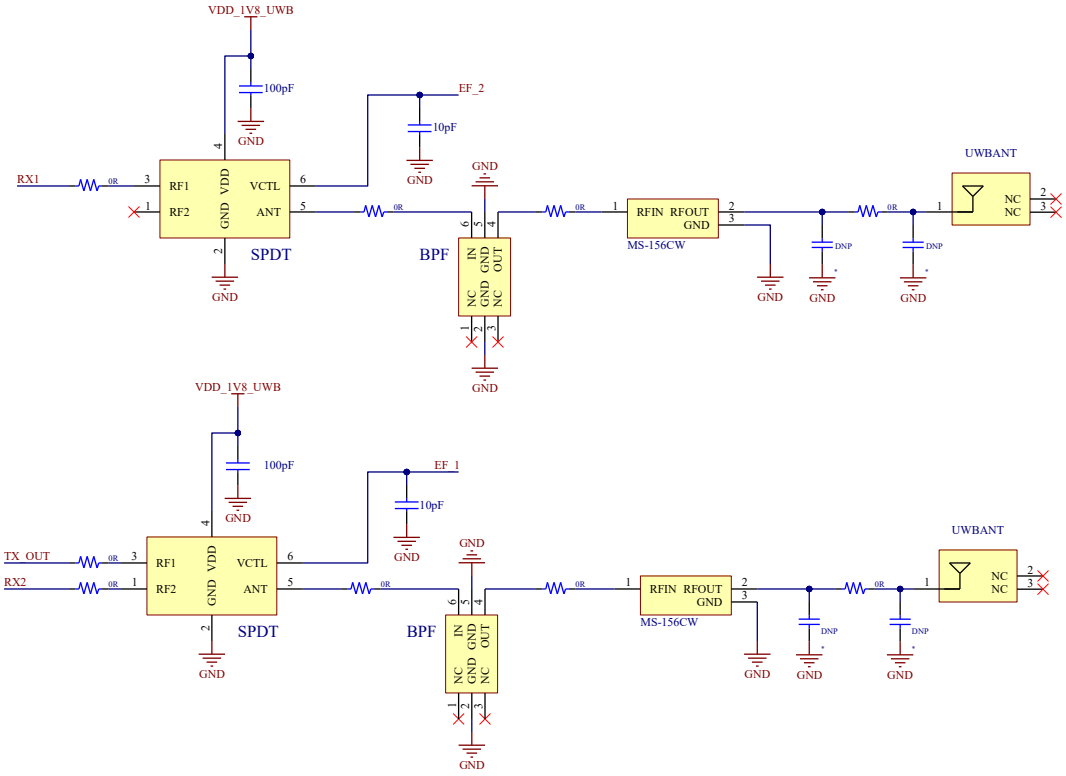


Figure 5 : UWB SR150 Module 2D AoA configuration

11. DCDC_EN

The DCDC_EN controls the power supply of the UWB IC.

Parameter		Test Condition	MIN	TYP	MAX	Unit
DCDC_EN	High level input voltage		0.8			V
	Low level input voltage				0.4	V

Table 9. DCDC_EN level

12. Application design-in information

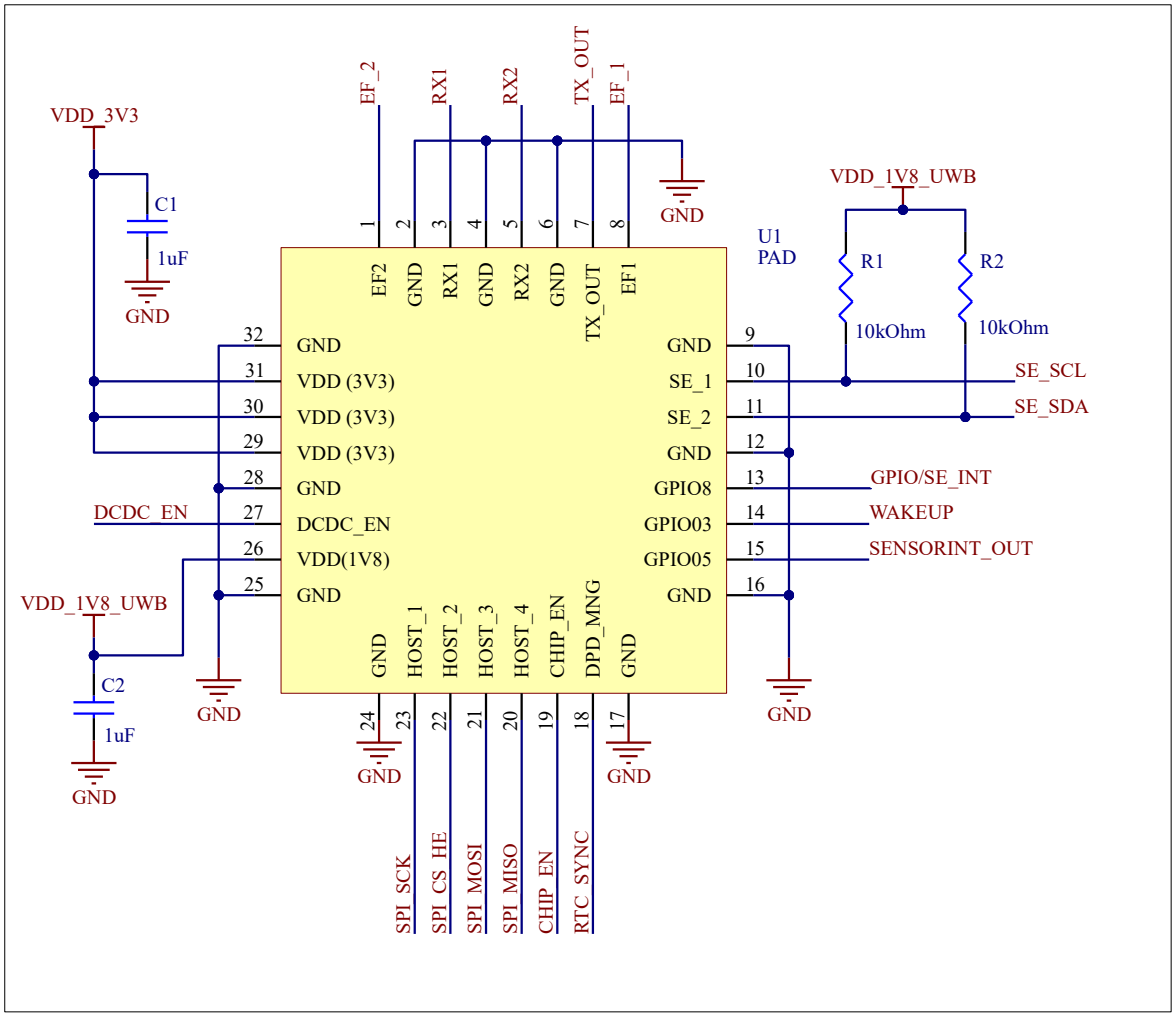


Figure 6 : UWB SR150 Module Reference Circuit

13. Module Package

13.1 Pinout Description

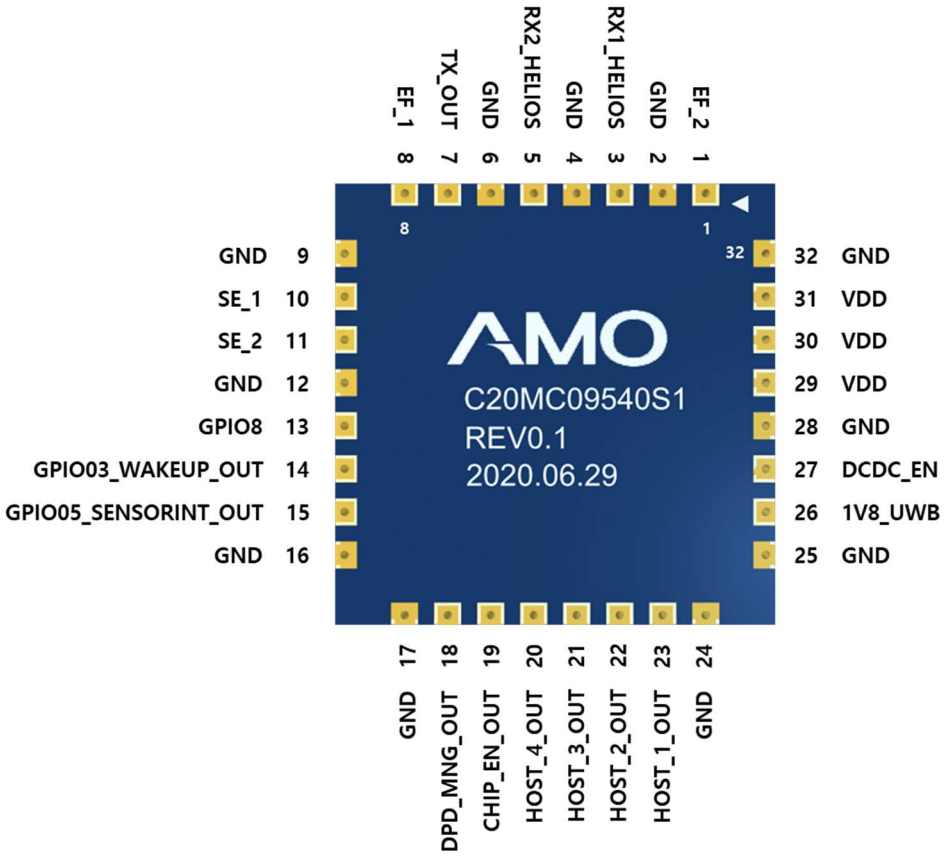


Figure 7 : Pin out Description(Bottom View)

13.2 Pin Description Box

PIN	PIN Name	PIN Type	Description
P1	EF_2	O	External front-end Control 2
P2	GND	G	Ground supply
P3	RX1_HELIOS	I	RX1 IN
P4	GND	G	Ground supply
P5	RX2_HELIOS	RX	RX2 IN
P6	GND	G	Ground supply
P7	TX_OUT	O	TX OUT
P8	EF_1	O	External front-end Control 1
P9	GND	G	Ground supply
P10	SE_1	I/O	clock for the secure element I2C interface
P11	SE_2	I/O	SDA connection for secure element I2C interface
P12	GND	G	Ground supply
P13	GPIO8	I/O	GPIO8
P14	GPIO03_WAKEUP	I/O	Host wakeup
P15	GPIO05_SENSORINT	I/O	GPIO05
P16	GND	G	Ground supply
P17	GND	G	Ground supply
P18	DPD_MNG	I/O	Deep Power Down control
P19	CE	I/O	connection for disabling/ enabling the chip
P20	HOST_4	I/O	MISO connection for the SPI host interface
P21	HOST_3	I/O	MOSI connection for the SPI host interface
P22	HOST_2	I/O	Slave select connection for the SPI host interface
P23	HOST_1	I/O	clock for the SPI host interface
P24	GND	G	Ground supply
P25	GND	G	Ground supply
P26	1V8_UWB	P	1.8V RF Switch Power output
P27	DCDC_EN	I	DC/DC Enable control
P28	GND	G	Ground supply
P29	VDD	P	3.3V Power supply
P30	VDD	P	3.3V Power supply
P31	VDD	P	3.3V Power supply
P32	GND	G	Ground supply

Table 10. Pin Description

13.3 Module Dimension or Footprint

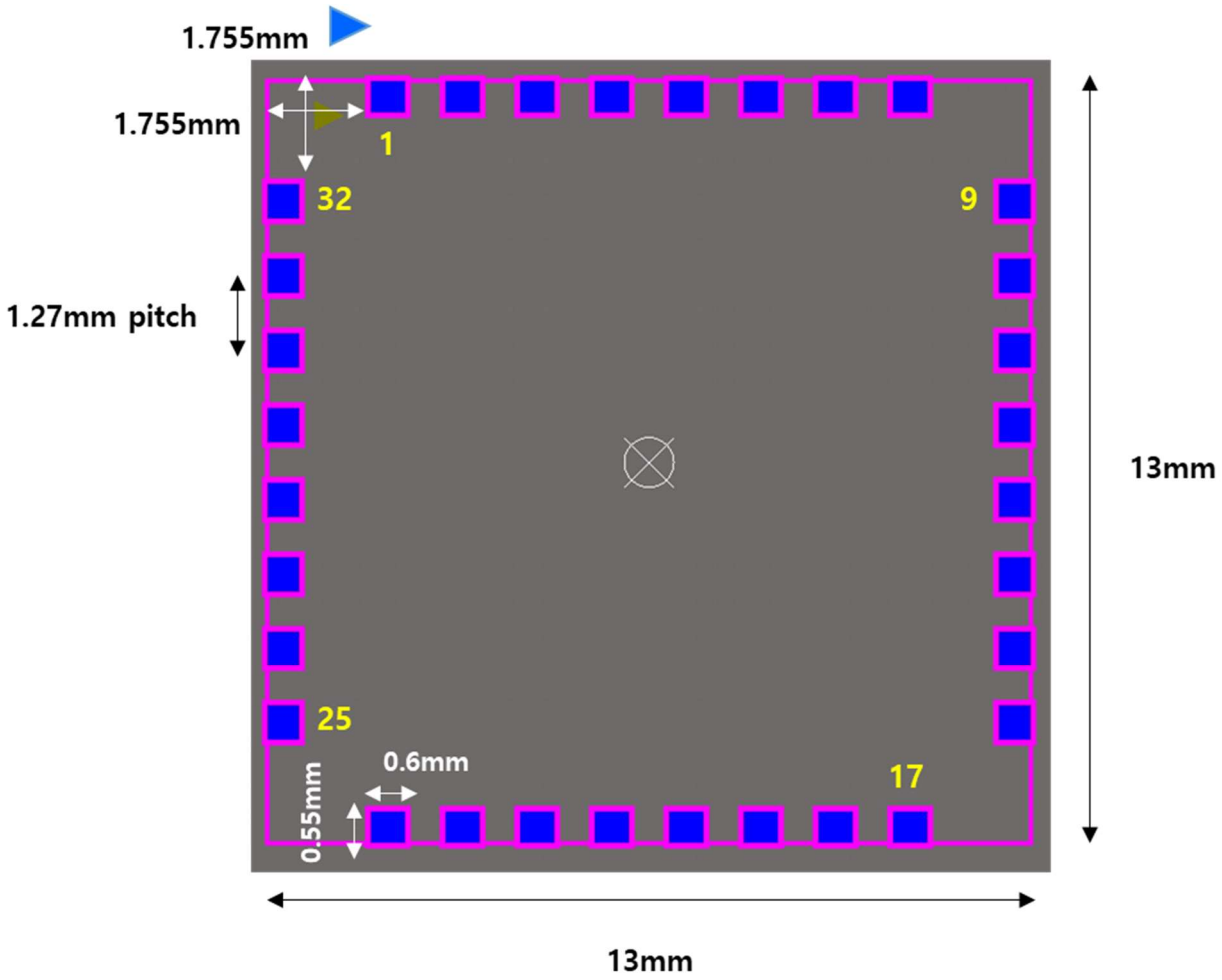


Figure 8. Pin Dimension or Footprint (TOP View)

14. Packing

Description	Data
Module Dimension	13mm*13mm*2.7mm
Reel Carrier Pocket	24W*20P
Reel Cover Tape	21.3mm*480m
Module Quantity	1K

Table 11. Reel Packing Description

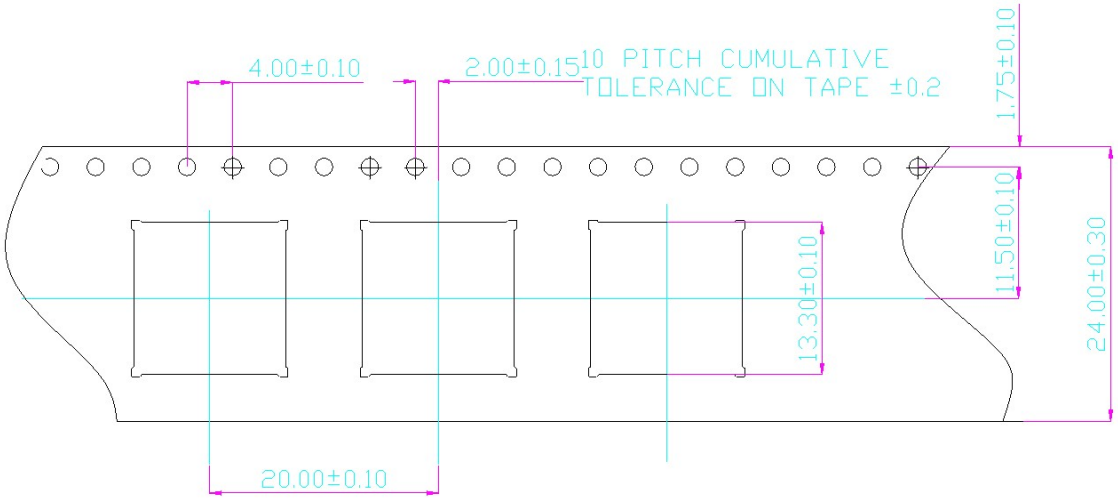


Figure 9. Reel Packing

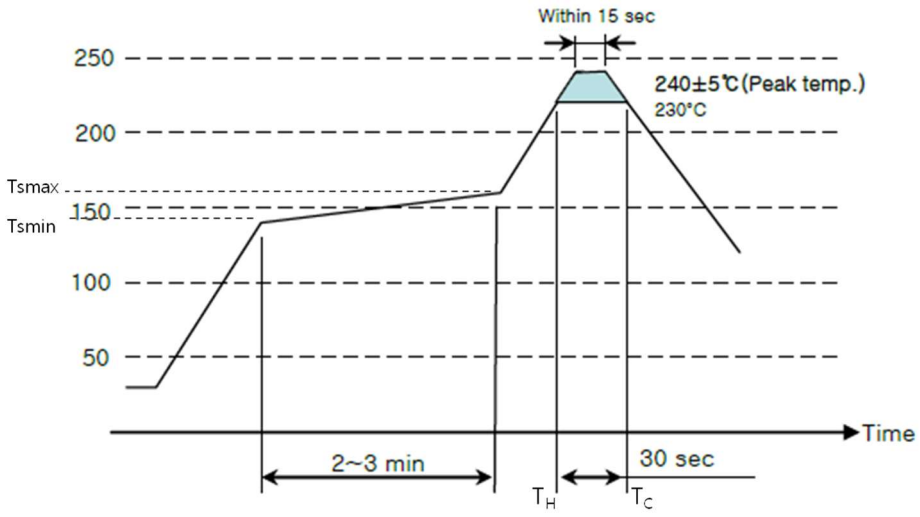
15. Soldering Condition

7.1 Manual Soldering – Pb Free

① Soldering Temperature: 360℃ ± 5℃, 5sec max.
(Solder : Sn /Ag /Cu : 96.5 /3.0 /0.5)

② Moisture sensitivity precautions, as indicated on the packing, must be respected at all times

7.2 Recommended Reflow Condition – Pb Free



Profile Feature	Pb-Free Assembly
Preheat -Temperature Min (T_{smin}) -Temperature Typical ($T_{stypical}$) -Temperature Max (T_{smax}) -Time T_{smin} to T_{smax}	 -140˚C -150˚C -160˚C -2 ~ 3 min
Peak Temperature	240±5˚C
Time of actual peak temperature	Max. 15 seconds

Heating to Cool	
-Temperature Heating (T_H)	-230˚C
-Temperature Cool (T_C)	-230˚C
-Time T_H to T_C	-30 seconds

16. Glossary

Abbreviation	Long term
AoA	Angle of arrival
DPD	Deep Power Down
HPD	Hard Power Down
HRP	High Rate Pulse Repetition Frequency
NC	Not Connected
OTP	One Time Programmable
PMU	Power Management Unit
RF	Radio Frequency
RSSI	Received Signal Strength Indicator
RTLS	Real-time locating systems
RX	Receiver
SFD	Start of Frame Delimiter
SNR	Signal to Noise Ratio
SPI	Serial Peripheral Interface
STS	Secure Training Sequence
SWD	Serial Wire Debug
TDoA	Time Difference Of Arrival
ToF	Time of Flight
TX	Transmitter
UART	Universal Asynchronous Receiver and Transmitter